What is Claimed is:

1. A nonvolatile ferroelectric memory device having a multi-bit control function, comprising:

a plurality of memory cells connected to a plurality of bitlines to be activated simultaneously;

a plurality of column selecting switches connected one by one to the plurality of bitlines;

a common data bus unit connected in common to the plurality of column selecting switches; and

a sense amplifier for comparing a reference voltage level with a voltage level of averaged data applied through the common data bus unit and amplifying the comparison result,

wherein the averaged data is average of charge values applied from the plurality of memory cells via the plurality of column selecting switches.

2. The device according to claim 1, wherein the plurality of data are the same data.

3. The device according to claim 1, wherein each memory cell comprises a switching device and a nonvolatile ferroelectric capacitor,

the switching device is connected between a bitline and a first electrode of the nonvolatile ferroelectric capacitor, and

a second electrode of the nonvolatile ferroelectric capacitor is connected to a plateline.

4. The device according to claim 3, wherein the plurality of memory cells are arranged vertically and horizontally, and

a pair of bitlines are connected to the same wordline and the same plateline.

5. A nonvolatile ferroelectric memory device having a multi-bit control function, comprising:

a plurality of cell array blocks to be activated simultaneously, comprising a plurality of column selecting switches connected one by one to a plurality of main bitlines;

a common data bus unit connected in common to the plurality of cell array blocks; and

a plurality of sense amplifiers for comparing reference voltage levels with voltage levels of a plurality of averaged data applied through the common data bus unit and amplifying the comparison data to output multi-bit data

having different voltage levels;

wherein the plurality of cell array blocks are arranged side by side at a half side divided by the common data bus unit.

6. The device according to claim 5, wherein the plurality of averaged data are averages of charge values applied from the plurality of cell array blocks.

7. The device according to claim 6, wherein the plurality of data applied from the plurality of cell array blocks to one sense amplifier are the same data.

8. The device according to claim 5, wherein each of the plurality of cell array blocks further comprises a plurality of main bitline sensing load units for selectively providing power voltage to the plurality of main bitlines to control sensing load of the main bitlines.

9. The device according to claim 5, wherein each of the plurality of cell array blocks applies a number of 2^m write voltages to memory cells to write m bit data in a write mode.

10. The device according to claim 5, wherein each of the plurality of sense amplifiers compares and amplify a number of 2^m-1 reference voltage levels with the plurality of averaged data when m bit data are sensed in a write mode.

11. The device according to claim 5, further comprising:

a data encoder for encoding the multi-bit data having a plurality of different data levels to output n bit data into a data input/output bus;

a data decoder for decoding the n bit data applied from the data input/output bus; and

a digital/analog converter for converting a voltage level of data decoded in the data decoder into the common data bus unit.

12. The device according to claim 5, further comprising:

a timing data register array unit for storing data read in the plurality of cell array blocks through the common data bus unit in a read mode and storing input data in a write mode; and

a timing data buffer unit for buffering read data stored in the timing data register array unit and

outputting the input data into the timing data register array unit.

13. A nonvolatile ferroelectric memory device having a multi-bit control function, comprising:

a plurality of cell array blocks to be activated simultaneously, comprising a plurality of column selecting switches connected one by one to a plurality of main bitlines;

a common data bus unit connected in common to the plurality of cell array blocks; and

a plurality of sense amplifiers for comparing and amplifying different reference voltage levels with voltage levels of a plurality of averaged data applied from the plurality of cell array blocks and outputting multi-bit data having different voltage levels;

wherein the plurality of cell array blocks are arranged side by side at both half-sides divided by the common data bus unit.

14. The device according to claim 13, wherein the plurality of averaged data are averages of charge values applied from the plurality of cell array blocks.

15. The device according to claim 13, wherein the plurality of data applied from the plurality of cell array blocks to one sense amplifier are the same data.

16. The device according to claim 13, wherein each of the plurality of cell array blocks further comprises a plurality of main bitline sensing load units for selectively providing power voltage to the plurality of main bitlines in response to a main bitline control signal to control main bitline sensing load.

17. The device according to claim 13, wherein each of the plurality of cell array blocks applies a number of 2^m write voltages to memory cells sequentially to write m bit data in a write mode.

18. The device according to claim 13, wherein each of the plurality of sense amplifiers compares and amplify a number of 2^m-1 reference voltage levels with voltage levels of the plurality of averaged data when m bit data are sensed in a read mode.

19. The device according to claim 13, further comprising:

a data encoder for encoding the multi-bit data having a plurality of different data levels to output n bit data into a data input/output bus;

a data decoder for decoding n bit data applied from the data input/output bus; and

a digital/analog converter for converting voltage levels of data decoded in the data decoder into the common data bus unit.

20. The device according to claim 13, further comprising:

a timing data register array unit for storing data read in the plurality of cell array blocks through the common data bus unit in a read mode and storing input data in a write mode; and

a timing data buffer unit for buffering read data stored in the timing data register array unit, and outputting the input data into the timing data register array unit.